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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/862,941
Filing Date: May 22, 2001
Appellant(s): FLOOD, MARK

FLOOD, MARK
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/27/05 appealing from the Office action mailed 6/30/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect.

VI. C claims 8-12 should be claims 29, 35-37 and 47.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,199,169	Voth	12-1998
6,449,732	Rasmussen et al	12-1999
6,775,246	Kuribayashi et al	9-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-52 are presented for examination. These rejections are set forth in prior Office Action, Paper No. 09862,941 and reproduced for convenience.

Claim Rejections 35 USC § 102

1. The following is a quotation of appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United Stated before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-7, 13-28, 30-34, 38-46, 48-52,** are rejected under 35 U.S.C. 102(e) as being unpatentable over **Voth** (US Patent No. 6,199,169: System and method for synchronizing time across a computer cluster, Filed Dec. 15, 1998).

Regarding Claim 1, Voth discloses a time synchronization apparatus for synchronizing operation of a first controller with that of a second controller in a control system, the synchronization apparatus comprising:

a processor interface for interfacing the synchronization apparatus with a host processor; (see col. 4, lines 17-27)

a transmitter adapted to transmit synchronization information and data to a network in the control system; (see col. 2, lines 57-60)

a receiver adapted to receive synchronization information and data from the network; (see col. 2, lines 60-61) and

a timing system with a clock that maintains an indication of time according to information received from one of the network and the host processor. (see col. 2, lines 51-54)

Regarding Claim 2, Voth discloses the time synchronization apparatus of claim 1, being configurable to operate as one of a synchronization master and a synchronization slave. (see col. 4, lines 35-42)

Regarding Claims 3, 20, Voth discloses the time synchronization apparatus of claim 1, 14, being configured to operate as a synchronization master, wherein the transmitter periodically transmits message frames at a fixed period. (see col. 4, lines 43-47)

Regarding Claims 4, 15, Voth discloses the time synchronization apparatus of claim 3, 14, wherein the fixed period is about 50μs. (According to Applicant's specification on page 28 at lines 15-16, it states, *"...the synchronization component can transmit (broadcast) a frame every 50μs or some other fixed time period."* see Voth col. 4, lines 43-54; where the reference states that the update period is performed at a regular or periodic fixed time period which can be equal to 50us or some other time period.)

Regarding Claims 5, 16, Voth discloses the time synchronization apparatus of claim 3, 14, wherein the transmitter transmits a message frame having an LCM indicator at a least common multiple (LCM) interval. (see Voth col. 4, lines 43-54: *"...use a repeating update cycle...Update cycle...includes an initial calculation ... scheduling period...a time adjustment period."* Applicant's specification states on page 13 at lines 20-26 that *"...least common multiple (LCM) period, ...can be set to the lowest integer multiple of periodic tasks..."* (i.e. set to 1) Thus, LCM is tied to reference's periodic update cycle.)

Regarding Claims 6, 17, Voth discloses the time synchronization apparatus of claim 5, 16, wherein the LCM interval is 600ms. (see Voth col. 4, lines 43-54: *"...use a repeating update cycle...Update cycle...includes an initial calculation...scheduling period...a time*

adjustment period." Applicant's specification status on page 13 at lines 20-26 that *"...600ms is exemplary... other LCM periods fall within the scope of the present invention..."* Thus, LCM is equal to periodic update cycle.)

Regarding Claims 7, 30, Voth discloses the time synchronization apparatus of claim 3, 14, being configured as a synchronization master, wherein the transmitter transmits message frames having multiplexed data and direct data. (see col. 3, lines 1-9)

Regarding Claim 13, Voth discloses the time synchronization apparatus of claim 7, wherein the timing system is adjustable according to information received from the host processor. (see col. 2, lines 51-54)

Regarding Claim 14, Voth discloses the time synchronization apparatus of claim 1, being configured as a synchronization slave, wherein the receiver receives message frames at a fixed period, and wherein the timing system is adjusted according to the fixed period. (see col. 4, lines 43-47)

Regarding Claim 18, Voth discloses the time synchronization apparatus of claim 16, wherein the timing system is adjusted according to the LCM indicator. (see col. 4, lines 47-44)

Regarding Claim 19, Voth discloses the time synchronization apparatus of claim 16,

wherein the receiver interrupts the host processor according to the LCM indicator. (see col. 4, lines 43-47)

Regarding Claim 21, Voth discloses the time synchronization apparatus of claim 20, wherein the message frames received and transmitted by the receiver and transmitter, respectively, comprise multiplexed data and direct data. (see col. 5, lines 18-25)

Regarding Claims 22, 43, Voth discloses the time synchronization apparatus of claim 21, 39, wherein the data field comprises 6 32 bit words, and wherein the amount of multiplexed data and the amount of direct data in each message frame is configurable. (see col. 5, lines 50-59; col. 6, lines 10-14: *"Different implementations of the present invention may use difference sizes for an, or all, of these components."*, where reference states that different sizes and values (i.e. amounts of data: 32 bit words) can be used for the data contained within message frames and therefore is configured by implementation.)

Regarding Claim 23, Voth discloses the time synchronization apparatus of claim 22, wherein each message frame comprises a direct data portion and a multiplexed data portion, wherein the direct data comprises the direct data portion of a single frame, and wherein the multiplexed data comprises the multiplexed data portions of a plurality of frames. (see col. 5, lines 18-25)

Regarding Claim 24, Voth discloses the time synchronization apparatus of claim 23, wherein the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame. (see col. 5, lines 26-29; col. 5, lines 50-59)

Regarding Claims 25, 26, Voth discloses the time synchronization apparatus of claim 24, wherein the receiver presents direct data or multiplexed data from received message frames to the host processor at the fixed or a multiple of the fixed period. (see col. 4, line 67 - col. 5, line 5)

Regarding Claim 27, Voth discloses the time synchronization apparatus of claim 14, comprising a multiplier receiving an operand from the receiver, a multiplication value on the host processor, and providing a multiplication result value to at least one of the host processor and the transmitter, wherein the multiplication result value is the product of the multiplication value and the operand. (see col. 5, lines 18-20)

Regarding Claims 28, 32, Voth discloses the time synchronization apparatus of claim 27, 30, wherein the direct data received in the message frame comprises the operand. (see col. 5, lines 18-25)

Regarding Claim 31, Voth discloses the time synchronization apparatus of claim 30, wherein at least a portion of the direct data in the message frames transmitted by the

transmitter is provided to the transmitter by the receiver, wherein the direct data from a received message frame is passed through to the transmitter. (see col. 6, lines 31-37)

Regarding Claims 33, 34, Voth discloses the time synchronization apparatus of claim 30, wherein at least a portion of the direct data and multiplexed data in the message frames transmitted by the transmitter is provided to the transmitter by the host processor. (see col. 5, lines 20-25)

Regarding Claim 38, Voth discloses a synchronization module in a control chassis for synchronizing operation of a first controller in the control chassis with that of a second controller outside the control chassis, comprising:

a host processor in communication with the first controller via a backplane bus in the control chassis; (see col. 4, lines 17-27)

a transmitter adapted to transmit synchronization information and data to a network in the control system; (see col. 2, lines 57-60)

a receiver adapted to receive synchronization information and data from the network; (see col. 2, lines 60-61)

a timing system with a clock and maintaining an indication of time according to information received from one of the network and the host processor; (see col. 2, lines 51-54) and

a synchronization circuit operatively associated with the host processor, the transmitter, the receiver, and the timing system, and configurable by the host

processor to operate the module as one of a synchronization master and a synchronization slave. (see col. 4, lines 35-42)

Regarding Claim 39, Voth discloses a synchronization circuit for synchronizing operation of a first controller with that of a second controller in a control system, comprising:

a processor interface for interfacing the synchronization circuit with a host processor; (see col. 4, lines 17-27)
a transmitter component adapted to transmit synchronization information and data to a network in the control system; (see col. 2, lines 57-60)
a receiver component adapted to receive synchronization information and data from the network; (see col. 2, lines 60-61) and
a timing system with a clock and maintaining an indication of time according to information received from one of the network and the host processor, wherein the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave. (see col. 2, lines 51-54)

Regarding Claims 40, 41, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames comprising direct data, and wherein the direct data is obtained from at least one of the receiver, the host

processor, and the multiplier. (see col. 5, lines 18-25)

Regarding Claim 42, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames comprising multiplexed data, and wherein the multiplexed data is obtained from the host processor. (see col. 4, lines 43-47)

Regarding Claim 44, Voth discloses the system of claim 39, wherein the receiver component periodically receives message frames comprising direct data, multiplexed data, and status information from the network, and wherein the synchronization circuit provides at least one of received direct data, received multiplexed date and received status information from the receiver component to the host processor. (see col. 6, lines 31-37)

Regarding Claim 45, Voth discloses the system of claim 44, further comprising a multiplier operating on the received direct data, and wherein the synchronization circuit provides a multiplier result value from the multiplier to the host processor. (see col. 5, lines 18-20)

Regarding Claim 46, Voth discloses the system of claim 45, wherein the synchronization circuit provides a multiplication value to the multiplier from the host processor. (see col. 5, lines 18-20)

Regarding Claim 48, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames comprising direct data, multiplexed data, and configuration information, and wherein the synchronization circuit provides at least one of the direct data, multiplexed data, and configuration information to the transmitter component from the host processor. (see col. 5, lines 18-25)

Regarding Claim 49, Voth discloses the system of claim 39, wherein the transmitter component periodically transmits message frames having synchronization information, wherein the synchronization information is obtained from the timing system, and wherein the timing system is adjusted according to at least one of synchronization information received from the network and synchronization information from the host processor. (see col. 4, lines 43-47; col. 2, lines 51-54)

Regarding Claim 50, Voth discloses the system of claim 39, wherein the synchronization circuit interrupts the host processor according to receipt of an LCM indicator by the receiver. (see col. 4, lines 43-47)

Regarding Claim 51, Voth discloses the system of claim 39, wherein the synchronization circuit interrupts the host processor periodically for presentation of at least one of direct data and multiplexed data from the receiver to the host processor. (see col. 4, lines 43-47)

Regarding Claim 52, Voth discloses a synchronization system for synchronizing a first controller with a second controller in a control system, comprising:

means for interfacing the synchronization circuit with a host processor; (see col. 4, lines 17-27)

means for transmitting synchronization information and data to a network in the control system; (see col. 2, lines 57-60)

means for receiving synchronization information and data from the network; (see col. 2, lines 60-61) and

means for maintaining an indication of time according to information received from one of the network and the host processor, wherein the synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave. (see col. 2, lines 51-54)

Claim Rejection 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 8, 9, 10, 11, 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Voth et al.** (US Patent No. 6,199,169) in view of **Ramussen et al.** (US Patent No. 6,449,732: Method and apparatus for processing control using a multiple redundant processor control system).

Regarding Claim 8, Voth discloses a header with flag bytes, a control byte and a data field and a bitmask used in error detection for data within the message frames. Voth does not disclose specifically the CRC technique in error detection procedures. However, Rasmussen discloses the time synchronization apparatus of claim 7, wherein the same comprises three flag bytes, a control byte, a data field comprising the multiplexed data and the direct data, and two CRC bytes. (see Rasmussen col. 14, lines 1-4: *"Calculates and check the received CRCs..."* ; col. 14, lines 16-19: *"Calculates and send the transmit CRCs..."*)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Voth with the error detection capabilities as taught by Rasmussen. One of ordinary skill in the art would be motivated to modify Voth to employ the invention of Rasmussen in order to enhance the processing of time synchronization information with an extension in error detection capabilities. (see Rasmussen col. 5, lines 24-27: *"...hardware loop-back fault detection, CRC checking...."*)

Regarding Claims 9, 12, Voth discloses the time synchronization apparatus of claim 8, wherein the data field comprises 6 32 bit words, and wherein the amount of multiplexed data and the amount of direct data in each message frame is configurable. (see col. 5, lines 50-59; col. 6, lines 10-14: *"Different implementations of the present invention may use difference sizes for an, or all, of these components."*, where reference states that different sizes and values (i.e. amounts of data: 32 bit words) can be used for the data contained within message frames and therefore is configured by implementation.)

Regarding Claim 10, Voth discloses the time synchronization apparatus of claim 9, wherein each message frame comprises a direct data portion and a multiplexed data portion, wherein the direct data comprises the direct data portion of a single frame, and wherein the multiplexed data comprises the multiplexed data portions of a plurality of frames. (see col. 5, lines 18-25)

Regarding Claim 11, Voth discloses the time synchronization apparatus of claim 10, wherein the multiplexed data portion comprises configuration information indicative of the amount of multiplexed data and the amount of direct data in each message frame. (see col. 5, lines 26-32; col. 5, lines 48-59)

5. **Claims 29, 35, 36, 37, 47** are rejected under 35 U.S.C. 103(a) as being unpatentable over Voth et al. (US Patent No. 6,199,169) in view of **Kuribayashi et al.**

(US Patent No. 6,775,246: Method of determining master and slaves by communication capability of network nodes).

Voth discloses a time synchronization apparatus with designated master and slave nodes and a timing system with a periodic and continuously updating feature. (see Voth col. 35, lines 45: *"... a distributed system that maintains the synchronization between time clocks ..., one of the nodes...assumes a master role. The remaining nodes 102 then function as slaves ...To synchronize time clocks 212, master node 102a and slave nodes 102b-d use a repeating update cycle ...."*)

Regarding Claims 29, 47, Voth does not disclose an apparatus to process status information from an upstream device. However, Kuribayashi discloses the time synchronization apparatus of claim 14, 44, wherein the message frame comprises a status component indicative of the status of an upstream device and error counter, wherein the receiver provides the status component to the host processor. (see Kuribayashi col. 2, lines 9-19; col. 8, lines 37-42)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Voth with an apparatus to process status information from an upstream device as taught by Kuribayashi. One of ordinary skill in the art would be motivated to employ the invention of Kuribayashi in order to extend the processing of time synchronization information to control the operation of additional devices. (see Kuribayashi col. 1, lines 53-57: *"...provide a novel communication control apparatus, which permits the proper and simple setting of transmission/reception*

nodes...synchronization information in a high-speed network.")

Regarding Claim 35, Voth does not disclose a procedure to process a status signal from an upstream device in a daisy-chain. However, Kuribayashi discloses the time synchronization apparatus of claim 1, being configured as an intermediate node in a daisy-chain topology, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain. (see Kuribayashi col. 2, lines 9-19; col. 8, lines 37-42)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Voth in order for an apparatus to process status information from an upstream device as taught by Kuribayashi. One of ordinary skill in the art would be motivated to employ the invention of Kuribayashi in order to extend the processing of time synchronization information controlling the operation of networked devices. (see Kuribayashi col. 1, lines 53-57: *"...provide a novel communication control apparatus, which permits the proper and simple setting of transmission/reception nodes ...synchronization information in a high-speed network."*)

Regarding Claim 36, Voth discloses the time synchronization apparatus of claim 35, wherein the receiver receives message frames at a fixed period, and wherein the transmitter transmits message frames at the fixed period comprising direct data and multiplexed data. (see col. 4, lines 47-54)

Regarding Claim 37, Voth discloses the time synchronization apparatus of claim 36, wherein at least a portion of the direct data in the message frames transmitted by the transmitter is provided to the transmitter by the receiver, wherein the direct data from a received message frame is passed through to the transmitter. (see col. 4, lines 47-54)

Summary of Prior Art

. **Voth** (6,199,169) discloses a time synchronization system for a set of time clocks within a distributed network environment with master slave designations for connected systems (i.e. a first and a second) with time resolutions in the microsecond range.

. **Kuribayashi** (6,449,732) discloses the capability to transmit and receive time synchronization information and non synchronization data over the interconnected network.

. **Rasmussen** (6,775,246) discloses a time synchronization system that enable CRC error detection techniques.

(10) Response to Argument

A. As to claims **1 - 7, 13 - 28, 30 - 34, 38 - 46 and 48 - 52**, applicant argues in substance that:

A.1. The referenced prior art does not disclose " ... a processor interface for interfacing the synchronization apparatus with a host processor, a second controller, and a network in the control system ... " (see Appeal Brief Page 5, Lines 26-28)

A.2. The referenced prior art does not disclose " a transmitter adapted to transmit synchronization information and data to a network in the control system ". (see Appeal Brief Page 5, Lines 29-31) and (see Appeal Brief Page 8, Lines 17-18)

A.3. The referenced prior art does not disclose " a first controller in the control chassis with that of a second controller outside the control chassis ". (see Appeal Brief Page 7, Lines 21-22)

A.4. Applicant argues that the referenced prior art does not disclose " ... synchronization circuit is configurable by the host processor to operate as one of a synchronization master and a synchronization slave ... "(see Appeal Brief Page 8, Lines 9-10)

B. As to Claims **8 - 12**, applicant argues in substance that:

B.1. Applicant argues that the referenced prior art is non-analogous art. (see Appeal Brief Page 9, Lines 26-28; page 9, line 31 - page, line 3)

B.2. The referenced prior art does not disclose the capability to " function within convention industrial control system network environments and is therefore not "particular pertinent to the particular problem with which the inventor was concerned

". (see Appeal Brief page 11, lines 3-5)

C. As to claim **29, 35-37, 47,** applicant argues in substance that:

C.1. The referenced prior art does not disclose " ... receiving synchronization information from an upstream device in the daisy chain, transmitting the synchronization information to at least one downstream device ... ". (see Appeal Brief Page 11, Lines 21-24)

Examiner Response to Argument dated December 27, 2005

The examiner's rejection is proper given that the cited passages of Voth, Rasmussen, and Kuribayashi disclose the applicant's claimed invention.

As to point A.1:

Voth discloses a structural relationship analogous to the invention's claim limitations. Voth discloses a system consisting of at least 2 processors, one processor dedicated (i.e. a specified by parameter for a particular usage of processor) to the time synchronization process and a second processor dedicated (i.e. setup parameter for a process) to other computer related processes of system. An interprocessor interface exists between processors. And, the computer systems consists of two network adapters (i.e. network interfaces configurable via system configuration tool). One network adapter dedicated to the time synchronization process and the other network adapter dedicated to other computer processes. The other computer processes are the processes encompassed by the industrial process

which is utilizing the time synchronization service.

This configuration for the UNIX-like system (see Voth col. 4, lines 5-16: UNIX ; col. 4, lines 17-27: configuration), which utilizes standard well known in the art features, is analogous to applicant's invention. A processor interface (see Remarks dated December 27, 2005 page 6, lines 20-21: " a processor interface for interfacing the synchronization apparatus with a host processor ") exists between the time synchronization processor and the host (i.e. industrial processor). A bus structure exists for the two processors and the two network adapters, which is the backplane bus. Voth has a separate structure to accomplish the time synchronization function and a separate structure to accomplish the industrial control functions. Voth discloses that two systems or nodes are time synchronized. (see Voth col. 4, lines 17-27) A second UNIX type time synchronization system configured as above discloses the second controller. Voth discloses a network environment for the operation of the time synchronization system. (see Voth col. 4, lines 17-19)

As to point A.2:

Not only one skilled in the art knows the concept of data and non-data transfers between networked connected systems, but also, Voth discloses the same concept inherently as above (see Voth col. 2, lines 10-13). Although, Voth discloses the transmission of messages (i.e. data) between network connected systems in order to respond with a better explanation to remarks, the explicit disclosure of Kuribayashi prior art was introduced. Thus, the response for claim 1 remained as

(see Voth col. 2, lines 57-61) in page 4 of the Final Action.

Voth in view of Kuribayashi discloses the capability to transmit time synchronization information and non time synchronization data over an interconnected network. (see Kuribayashi col. 8, lines 29-34; col. 9, lines 2-4: clock signals (i.e. time synchronization information) and transmitting and receiving data (i.e. non time synchronization data))

Voth discloses the capability to transmit time synchronization information and non synchronization data over a network environment. As a further disclosure, Voth in view of Kuribayashi discloses the capability to transmit time synchronization information and non time synchronization data over an interconnected network. (see Kuribayashi col. 8, lines 29-34; col. 9, lines 2-4: clock signals (i.e. time synchronization information) and transmitting and receiving data (i.e. non time synchronization data))

As to point A.3:

Voth discloses that two systems or nodes are time synchronized. (see Voth col. 4, lines 17-27) A second UNIX type time synchronization system configured as above discloses the second controller (i.e. a separate system in its own chassis).

As to point A.4:

Voth discloses that one node assumes master status (see Voth col. 4, lines 37-38: master node) and is configured to perform the master node time synchronization

type functions. (see Voth col. 10, lines 44-45; col. 10, lines 53-55; col. 13, lines 61-62; col. 14, lines 9-10: configuration of master node)

As to point B.1:

Voth discloses a time synchronization system. (see Voth col. 2, lines 51-53: time synchronization system), the Rasmussen discloses a time synchronization system (see Rasmussen col. 4, lines 57-59; col. 12, lines 31-35), and Kuribayashi discloses a time synchronization system. Applicant's invention discloses a time synchronization apparatus. Therefore, Voth is analogous art and legitimate prior art and is utilized to disclose the applicant's invention.

As to point B.2:

Voth discloses a time synchronization system utilizing UNIX type system. The dedicated processor utilized within the time synchronization system is loaded only with the required operating system features. The communications network utilized is a very high speed capable network and the communications speeds in the communications network are within the invention's specification. Therefore, these features (i.e. high speed communications, operating system loaded only with required features) make the prior art disclosure of the invention possible and operable. (see Voth col. 4, lines 19-21: high speed network)

As to point C.1:

Voth discloses the usage of any number of different types of network and configurations (see Voth col. 4, lines 17-21), such as a star configuration or in a daisy chain configuration. Voth and Kuribayashi discloses the capability to send and receive information in a daisy-chain topology, the receiver receiving synchronization information from an upstream device in the daisy-chain, and the transmitter transmitting the synchronization information to at least one downstream device in the daisy-chain. (see Kuribayashi col. 2, lines 9-19; col. 8, lines 37-42)

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Kyung H. Shin KHS.

March 16, 2006

Conferees:

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